8. (Amended) A method for resolution enhancement in an analog to digital converter comprising the steps of:

converting a reference voltage of more than a least significant bit;

subtracting a mathematically-derived reference voltage of more than a least significant bit from the circuit's input voltage; and then

adding the converted reference voltage of more than a least significant bit to the converted reduced input voltage.

REMARKS

Drawings:

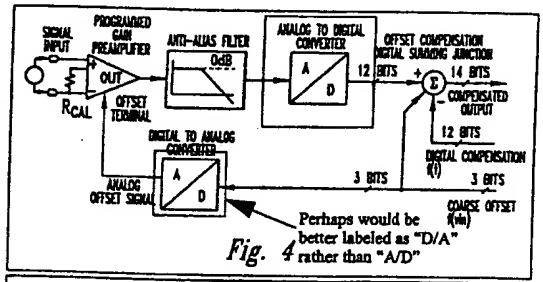

Fig. 4

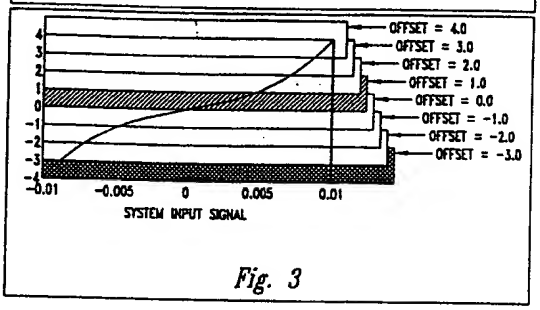

Fig. 3

The analog to digital converter is the top block labeled "A/D" in figure4 and the hysteresis referred to is a mathematical operation shown schematically by figure 3. There is not a dedicated hardware item which performs the hysteresis function. Hysteresis is applied as part of the coarse

offset which originates as part of the device's digital controls. Note that in figure 4 there are three bits controlling coarse offset. These three bits correspond to the eight levels of offset illustrated in figure3, since $2^3 = 8$ as originally discussed in the patent application's opening remarks.

Figure 4 shows two blocks labeled "A/D." Customarily, "A/D" refers to an analog to digital conversion function. One of the blocks shown in figure 4 is in reality a digital to analog converter, customarily referred to as "D/A." This typographical error is possibly confusing to those seeing the figure for the first time.

By way of further explanation, the hysteresis function is provided for those situations in which the signal being processed is just on the edge of transitioning from one offset range into an adjacent offset range: Suppose hysteresis was not provided. The offset ranges would not overlap as shown in figure 3, but would rather abut one another. In this case, should a signal make a transition from one offset range into the adjacent offset range and then for whatever reason quickly transition back into its original offset range (which could easily be the case for a signal "hovering" close to a range boundary), an undesirable effect of continuously switching ranges could occur. Providing hysteresis in which offset ranges overlap as shown in figure 3 eliminates this effect. Once the signal transitions into an adjacent offset range, it finds itself in the middle of this new range rather than on the range's edge as would be the case if hysteresis were not provided.

Claim Rejections – 35 U.S.C 112

Examiner's Comment:
Claims 7-8 contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 7 recounts the offset bands shown vertically displaced along figure 3's vertical axis.

Claim 8 summarizes the operation of the overall circuit: Resolution of this conversion scheme is enhanced by digitizing an input signal from which a DC component is subtracted. The numeric value of that DC component is then mathematically summed back in to the converted result which has the effect of increasing the apparent number of conversion bits.

Examiner's Comment:
It is not clear how overlapping the offset bands can provide the hysteresis as recited in line 6 of claim 7 since Fig. 3 of the present invention does not show any analog to digital converter and the hysteresis in combination with the offset bands.

Again, the basic idea behind hysteresis is that once an input signal transitions into an adjacent offset range, it finds itself in the middle of this new range rather than on the range's edge as would be the case if the ranges abutted rather than overlapped. Hysteresis prevents a signal from leaving an offset range until it crosses that range's boundary. Once it crosses a range boundary, it then finds itself in the middle of the adjacent range so that it cannot immediately return to the range from which it started. This presents continuous, undesirable range changes.

Examiner's Comment:
The method as recited in claim 8 is not described under detailed description of the invention of the present specification. It is just briefly described under Patent Literature from line 7 to line 18 of page 5 of the present specification.

Claim 8 is a summary of the proposed invention. Please see the remarks in the preceding paragraph.
Claims 1-2, 4-5, and 7-8 were indicated as indefinite in paragraph 5 of the Office Letter. Accordingly, the objections are believed addressed in the claims as now amended.

Further Response:

First, the word "span" in this context refers to the range of voltages which can be accommodated by the analog to digital converter block labeled "A/D" shown in Fig. 4. This "A/D" block must be distinguished from the digital to analog converter block unfortunately also labeled "A/D". The mark-ups on the above figures, hereby made of record, should clarify which is which.

Claims 1 and 2 describe the process of the circuit adapting itself to the particular transducer to which it is connected. For transducers having a relatively large output signal, the input preamplifier need have only relatively small gain to match the transducer output to the analog to digital converter block's span. Conversely, for transducers having a relatively small output signal, the input preamplifier need have a relatively large gain to match the transducer output to the analog to digital converter block's span.

Claims 4 and 5 identify the blocks shown in Fig. 4.
Claims 7 and 8 summarize the circuit's operation.

Claim Rejections 35 U.S.C. 103 (paragraph 7 of the Office Letter)

Claim 3 has been cancelled without prejudice.

Allowable Subject Matter

Claim 6 was indicated as allowable subject to being rewritten in independent form, which is accomplished by the present amendment.
Claims 1-2 and 4-5 have been amended as previously indicated to remove the objections under 35 U.S.C. 112 and are therefore allowable.
Claims 7 and 8 stood rejected under 35 U.S.C. 112 and have been amended in a manner believed to overcome the indefiniteness pointed out by the Examiner and are therefore believed allowable.
Applicant believes this application is now in condition for allowance, which Notice is respectfully solicited.

Please charge Deposit Account No. 02-2960 in the amount of 252.00. The Commissioner is hereby authorized to charge any additional fees, including fees for extension of time, which may be required at any time during the prosecution of this amendment without specific authorization, or credit any overpayment to Deposit Account 02-2960.

PETITION AND FEE FOR EXTENSION OF TIME
37 C.F.R. § 1.136(a)

The applicant petitions the Commissioner of Patents and Trademarks to extend the time for response to the Final Rejection dated February 13, 2002, for one month from April 13, 2002 to May 13, 2002.

Please charge the fee of $110.00 for 1 month to Deposit Account No. 02-2960. Please charge any necessary additional fees under 37 C.F.R. § 1.16 or § 1.17 or credit any overpayments to Deposit Account No. 02-2960.

Respectfully submitted,

Conrad O. Gardner
Registration No.: 22,2462
Telephone No.: (206) 655-5510

The Boeing Company
P.O. Box 3707, M/S 13-08
Seattle, WA 98124-2207

ATTACHMENT FOR SPECIFICATION AMENDMENTS

None.

ATTACHMENT FOR CLAIM AMENDMENTS

The following is a marked up version of amended claims 1, 4, 5, 6, 7, and 8 in which underlines indicate insertions and brackets indicate deletions.

1. (Twice Amended) An analog to digital converter resolution enhancement method comprising the steps of:

providing an analog to digital converter having an AC component less than or equal to one-half the [span] full range of signals which [of] the analog to digital converter itself can accommodate;

connecting the input signal to the input of a programmed gain preamplifier;

utilizing said programmed gain preamplifier to match the full range of said analog to digital converter to said AC component of the input signal; and then,

[complementing] enhancing the analog to digital conversion range of said analog to digital converter by an offset value thereby causing said programmed gain preamplifier to amplify the input signal at high gain while applying the offset value at low gain.

4. (Twice Amended) In combination:

a reduced span analog to digital converter;

a programmed gain preamplifier coupled between an input terminal for receiving an input signal and said reduced span analog to digital converter;

said programmed gain preamplifier having a high differential gain for said input signal and a low single-ended gain for the offset signal;

said programmed gain preamplifier matching the [span] range of signals which [of] said analog to digital converter can fully accommodate against only a portion of the signal present at the circuit's [system] input; and,

the entire range of [input] signals [range] provided by positioning the analog to digital converter's input signal range [span] by means of an offset value.

5. (Twice Amended) In combination:

[a] an analog to digital converter having an input terminal and an output terminal;

a programmed gain preamplifier having an input terminal for receiving an input signal, an offset terminal, and an output terminal;

a digital summing junction;

said output terminal of said analog to digital converter coupled to said digital summing junction;

an anti-alias filter having an input terminal and an output terminal;

said output terminal of said anti-alias filter coupled to said input of said analog to digital converter;

said input terminal of said anti-alias filter coupled to said output terminal of said programmed gain preamplifier; and,

said digital to analog converter coupled between said digital summing junction and said offset terminal of said programmed gain preamplifier for providing an analog offset signal to said programmed gain preamplifier.

6. (Twice Amended) The combination: [according to claim 5]

[wherein said programmed gain preamplifier provides a high differential gain for said input signal and a low single-ended gain for said analog offset signal.]

an analog to digital converter having an input terminal and an output terminal;

a programmed gain preamplifier having an input terminal for receiving an input signal, an offset terminal, and an output terminal;

a digital summing junction;

said output terminal of said analog to digital converter coupled to said digital summing junction;

an anti-alias filter having an input terminal and an output terminal;

said output terminal of said anti-alias filter coupled to said input of said analog to digital converter;

said input terminal of said anti-alias filter coupled to said output terminal of said programmed gain preamplifier;

said digital to analog converter coupled between said digital summing junction and said offset terminal of said programmed gain preamplifier for providing an analog offset signal to said programmed gain preamplifier; and,

wherein said programmed gain preamplifier provides a high differential gain for said input signal and a low single-ended gain for said analog offset signal.

7. (Amended) In the method of operating an analog to digital converter for resolution enhancement, the steps of:

displacing the [span] input signal range of the analog to digital converter [along the vertical axis] to one of a plurality of overlapping positions comprising [shaded] offset bands wherein the width of each band is representative of the [span] input signal range of the analog to digital converter; and,

overlapping the offset [bands] positions to provide hysteresis.

8. (Amended) A method for resolution enhancement in an analog to digital converter comprising the steps of:

converting a reference voltage of more than a least significant bit;

subtracting [the converted] a mathematically-derived reference voltage of more than a least significant bit from the circuit's input voltage; and then

adding the converted reference voltage of more than a least significant bit to the converted reduced input voltage.